AGM32 family System

1. System Overview

- RISC-V core with RV32IMAFC support
- 128KB SRAM
- 16KB instruction cache
- High speed XIP (execution in place) flash

2. Memory Map

	Address	
ROM	0x0001 0000 – 0x0001 1FFF	
System Control	0x0300 0000 – 0x0300 0FFF	
PLIC	0x0C00 0000 – 0x0C20 FFFF	
SRAM	0x2000 0000 – 0x2001 FFFF	
FLASH (XIP)	0x8000 0000 – 0x80FF FFFF	
Option bytes	0x8100 0000 – 0x8100 003F	
RTC	0x4000 0000 – 0x4000 007F	
FLASH control	0x4000 1000 – 0x4000 1FFF	
APB Peripherals	0x4001 0000 – 0x40FF FFFF	
AHB Peripherals	0x4100 0000 – 0x41FF FFFF	
External AHB	0x6000 0000 – 0x7FFF FFFF	

3. Clocks and Reset

4. Peripherals

4.1. APB peripherals

4.2. AHB peripherals

5. System Control

- Device boot mode (BOOT_MODE)
  - Address offset: 0x00

31 – 2	1	0
Reserved	BOOT_MODE	
	RO	RO

  - Bit [1:0]: Device boot mode

    The values of BOOT0 and BOOT1 pins are latched on the 4th rising edge of SYSCLK after a reset

- Reset control (RST_CNTL)
  - Address offset: 0x04
  - Bit 31 RSTF_LPWR: Reset flag by low power
    - 0: No reset detected
    - 1: Low power reset detected
  - Bit 30 RSTF_WDOG: Reset flag by watch dog
    - 0: No reset detected
    - 1: Watch dog reset detected
  - Bit 29 RSTF_IWDG: Reset flag by independent watch dog
    - 0: No reset detected
    - 1: Independent watch dog reset detected
  - Bit 28 RSTF_SFT: Reset flag by softare
    - 0: No reset detected
    - 1: Softare reset detected
  - Bit 27 RSTF_POR: Reset flag by power on reset
    - 0: No reset detected
    - 1: Power on reset detected
  - Bit 26 RSTF_PIN: Reset flag by NRST pin
    - 0: No reset detected
    - 1: NRST pin reset detected
  - Bit 25 RSTF_EXT: Reset flag by external logic
    - 0: No reset detected
    - 1: External logic reset detected
  - Bit 24 RST_REMOVE: Reset flag removal
    - Write 1 to clear all reset flags
  - Bit 1 RST_EXT_EN: External logic reset enable
    - 0: Exernal logic reset disabled
    - 1: External logic reset enabled
  - Bit 0 RST_SFT: Reset by software
    - Write 1 to trigger software reset
- Power control (PWR_CNTL)
  - Address offset: 0x08
  - Bit [1:0] LPWR_MODE: Low power mode
    - 00: Enter sleep mode with WFI (wait for interrupt) instruction
    - 01: Enter stop mode with WFI instruction
    - 11: Enter standby mode with WFI instruction
- Clock control (CLK_CNTL)
  - Address offset: 0x0C
  - Bit [15:12] SCLK_DIV_HIGH: Flash SPI clock divider high
    - Flash SPI clock is divided by (SCLK_DIV_HIGH + 1) from SYS_CLK, valid range is from 0 (divided by 1) to 15 (divided by 16)
  - Bit [11:8] SCLK_DIV_LOW: Flash SPI clock divider low
    - Must be set to the same value as SCLK_DIV_HIGH
  - Bit 6 PLL_RDY: PLL ready
    - 0: PLL is not ready
    - 1: PLL is ready

    - Bit 5 PLL_ON: PLL on
        - 0: PLL is turned off
        - 1: PLL is turned on
    - Bit 4 HSE_RDY: HSE ready
        - 0: HSE is not ready
        - 1: HSE is ready
    - Bit 3 HSE_BYP: HSE bypass
        - 0: HSE oscillator is not bypassed
        - 1: HSE oscillator is bypassed
    - Bit 2 HSE_ON: HSE on
        - 0: HSE oscillator is turned off
        - 1: HSE oscillator is turned on
- JTAG control (SWJ_CNTL)
    - Address offset: 0x14
    - Bit 4: NJTRST: Configuration for pin NJTRST
        - 0: NJTRST is used as a dedicated pin
        - 1: NJTRST is used as a user pin
    - Bit 3: JTDO: Configuration for pin JTDO
        - 0: JTDO is used as a dedicated pin
        - 1: JTDO is used as a user pin
    - Bit 2: JTDI: Configuration for pin JTDI
        - 0: JTDI is used as a dedicated pin
        - 1: JTDI is used as a user pin
    - Bit 1: JTMS: Configuration for pin JTMS
        - 0: JTMS is used as a dedicated pin
        - 1: JTMS is used as a user pin
    - Bit 0: JTCK: Configuration for pin JTCK
        - 0: JTCK is used as a dedicated pin
        - 1: JTCK is used as a user pin
- Debug control (DBG_CNTL)
    - Address offset: 0x1C
    - Bit 4 DBG_RTC_STOP: Stop RTC during debug
    - Bit 3 DBG_IWDG_STOP: Stop IWDG during debug
- Wake up rise triggers (WKP_RISE_TRG)
    - Address offset: 0x20
    - Bit [7:0] EXT_INT0–7: Wake up device from stop mode using EXT_INT0–7, rising edge triggered
    - Bit 8 ALARM: Wake up device from stop mode using RTC alaram
- Wake up fall triggers (WKP_FALL_TRG)
    - Address offset: 0x24
    - Bit [7:0] EXT_INT0–7: Wake up device from stop mode using EXT_INT0–7, falling edge triggered
    - Bit 8 ALARM: Wake up device from stop mode using RTC alaram
- Wake up pending register (WKP_PENDING)
    - Address offset: 0x28
    - Bits [8:0]: Correspoding bits are set when the selected triggering event occurs

- PBUS clock divider (PBUS_DIVIDER)
  - Address offset: 0x38
  - Bits [3:0] PBUS_DIV: APB clock is divided by (PBUS_DIV + 1) from SYS_CLK, valid range is from 0 (divided by 1) to 15 (divided by 16)
- APB peripheral reset (APB_RESET)
  - Address offset: 0x40
  - Each APB peripheral can be reset with the corresponding bit
    - 0: Reset is deasserted
    - 1: Reset is asserted
  - Bit [28]: I2C1
  - Bit [27]: I2C0
  - Bit [26]: CAN0
  - Bit [25]: UART4
  - Bit [24]: UART3
  - Bit [23]: UART2
  - Bit [22]: UART1
  - Bit [21]: UART0
  - Bit [20]: GPTIMER4
  - Bit [19]: GPTIMER3
  - Bit [18]: GPTIMER2
  - Bit [17]: GPTIMER1
  - Bit [16]: GPTIMER0
  - Bit [15]: TIMER1
  - Bit [14]: TIMER0
  - Bit [13]: GPIO9
  - Bit [12]: GPIO8
  - Bit [11]: GPIO7
  - Bit [10]: GPIO6
  - Bit [9]: GPIO5
  - Bit [8]: GPIO4
  - Bit [7]: GPIO3
  - Bit [6]: GPIO2
  - Bit [5]: GPIO1
  - Bit [4]: GPIO0
  - Bit [3]: SPI1
  - Bit [2]: SPI0
  - Bit [1]: WATCHDOG0
  - Bit [0]: FCB0
- AHB peripheral reset (AHB_RESET)
  - Address offset: 0x50
  - Each AHB peripheral can be reset with the corresponding bit
    - 0: Reset is deasserted
    - 1: Reset is asserted
  - Bit [3]: MAC0
  - Bit [2]: CRC0
  - Bit [1]: USB0

- Bit [0]: DMAC0

- APB peripheral clock enable (APB_CLKENABLE)
  - Address offset: 0x60
  - Clock must be enabled before any APB peripheral is accessed. Bit asssignment is the same as APB_RESET register
    - 0: Peripheral clock is disabled
    - 1: Peripheral clock is enabled
- AHB peripheral clock enable (AHB_CLKENABLE)
  - Address offset: 0x70
  - Clock must be enabled before any AHB peripheral is accessed. Bit asssignment is the same as AHB_RESET register
    - 0: Peripheral clock is disabled
    - 1: Peripheral clock is enabled
- APB peripheral clock stop during debug (APB_CLKSTOP)
  - Address offset: 0x80
  - Clock can be automatically stopped during debug for the following APB peripherals:
    - WATCHDOG
    - TIMER
    - GPTIMER
    - CAN
  - Bit asssignment is the same as APB_RESET register
    - 0: Clock is not stopped during debug
    - 1: Clock is stopped during debug
- Device ID code (DEVICE_ID)
  - Address offset: 0x100
  - Bit [31:0]: Returns the chip device ID: 0x40200001. Read only